REMARKS

Claims 16, 35, and 40-43 are pending in the present application. Claims 17-24 and 33-39 are canceled. Claim 16 is amended to incorporate the features previously presented in claims 38, and 39, since claim 39 is indicated as being allowable over the prior art. Reconsideration of the claims is respectfully requested.

I. Interview/Finality

On February 9, 2004, a telephone interview was conducted between the undersigned and Examiner Vinh Nguyen. Applicant argued that the finality of the Office Action issued December 9, 2003, was improper, because new grounds of rejection were applied to claims 18-24 and 35, but the new grounds of rejection were not necessitated by amendment. Although claims 18 and 35 were amended, these claims were only amended to be placed in independent form. Examiner admitted that claims 18-24 and 35 did not change in scope and that this fact was overlooked when the Office Action was made final. However, the Examiner refused to issue a new non-final Office Action without a written replay from Applicant. Applicant submits that the finality of the Office Action dated December 9, 2003, is improper and Applicant requests that the amendments made herein be entered and a new Office Action be issued based on these amendments.

II. 35 U.S.C. § 112, Second Paragraph

The Office Action rejects claim 39 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter, which applicants regard as the invention. This rejection is respectfully traversed.

With respect to claim 39, the Office Action states:

> In claim 39, it is unclear what "a current mirror" and "a plurality of transistors" represent. Are they shown in any of drawings? It appears that the term "the at least one transistor" has not been recited previously, therefore this term is indefinite. the same as "circuit component"? Furthermore, it is unclear how the current mirror and the plurality of transistors are interrelated and associated with the test circuitry in claim 18.

Office Action, dated December 9, 2003. Applicant respectfully disagrees. The "current mirror" and the "plurality of transistors" are supported by way of example and illustration in **Figure 10** and page 9, line 24, to page 10, line 7, of the present specification. As described in the instant disclosure, the current mirror **1000** distributes and equal amount of current to each of the plurality of transistors **1002**. However, the sum of the currents flowing through the plurality of transistors is passed through the diode-connected transistor **1008** responsive to a "FRY" signal **1006**. The high current flowing through the diode-connected transistor causes the diode-connected transistor to burn up, leaving a visible mark.

In view of the above, it is clear that the instant claims are definite and particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Therefore the rejection of claim 39 under 35 U.S.C. § 112, second paragraph is overcome. Furthermore, claim 16, which is amended to incorporate features previously presented in claim 39, also overcomes the rejection.

III. 35 U.S.C. § 102, Anticipation

The Office Action rejects claim 35 under 35 U.S.C. § 102 as being anticipated by *Nakata et al.* (US Patent No. 5,355,081). This rejection is respectfully traversed.

With respect to claim 35, the Office Action states:

> As to claims 35-36, Nakata et al disclose method for testing a plurality of integrated circuits (51) formed on a wafer as shown in figure 5. According to Nakata et al, as shown in figure 5, there is a network of signal paths (53,54) connect the integrated circuits to two or more connection points and each of the integrated circuits includes test circuitry (5,2,4,1) and each test circuitry (5,2,4,1) includes at least one visible component (light emitting diode "14") having an appearance.

Office Action, dated December 9, 2003. Applicant respectfully disagrees. Nakata teaches a method for testing a semiconductor integrated circuit having self testing circuits, wherein each self testing circuit includes a light emitting diode.

In contradistinction, the present invention provides a method for testing a circuit including a visible circuit component. When a circuit is defective, the present invention causes the visible circuit component to overheat. Claim 35 states:

35. A method of testing a circuit, comprising:

> applying at least one signal to testing circuitry;
> in response to a determination that the circuit is defective, modifying a visible circuit component in the circuit to have a different appearance, wherein modifying the visible circuit component includes causing the visible circuit component to **overheat.** [emphasis added]

Nakata does not teach or suggest testing a circuit component "wherein modifying the visible circuit component includes causing the visible circuit component to **overheat,**" as recited in claim 35. In fact, the Office Action does not address this feature with respect to claim 35. As such, the Office Action fails to establish a *prima facie* case of anticipation for claim 35. Since the applied reference fails to teach or suggest each and every claim limitation, claim 35 is not anticipated by *Nakata*.

Therefore, the rejection of claim 35 under 35 U.S.C. § 102 is overcome.

IV. 35 U.S.C. § 103, Obviousness

The Office Action rejects claims 16 and 40-43 under 35 U.S.C. § 103 as being unpatentable over *Nakata* in view of *Dukes et al.* (US Patent No. 5,570,035). Claim 16 is amended to incorporate the features of claim 39, which is indicated as being allowable over the prior art. Therefore, the rejection of claims 16 and 40-43 under 35 U.S.C. § 103 is overcome.

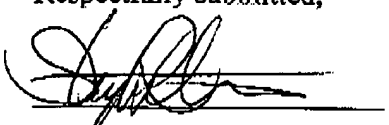
V. Conclusion

It is respectfully urged that the subject application is patentable over the prior art of record and is now in condition for allowance.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: February 9, 2004

Respectfully submitted,



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